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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER
COSTANZO, PATRICIA M

ART UNIT	PAPER NUMBER
2811	6

DATE MAILED: 06/03/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/821,546	LEE ET AL.	
	Examiner	Art Unit	
	Patricia M. Costanzo	2811	

-- The MAILING DATE of this communication appears on the cov r sheet with the correspondenc addr ss --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on *22 March 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 - 41* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 - 41* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 March 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *3* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Election/Restrictions

1. Applicant's traversal in Paper No. 5, filed March 22, 2002 is acknowledged. The restriction requirement is withdrawn.

Specification

2. The disclosure is objected to for the reasons that follow.

The last four lines on page 10 of the present Application state, in part, ". . . a new method of forming a chip scale package (CSP) where the I/O ball connections are directly mounted on the chip through vias formed in a next level of substrate" It is not clear to Examiner how the I/O ball connections can be "directly" mounted on the chip, when they are mounted on the chip "through vias formed in a next level of substrate".

The first sentence on page 11 states that the substrate is mounted, but fails to inform the reader, onto what is the substrate mounted?

Page 14, line 9 – does Applicant mean for "encapsulated (300)" to be "encapsulated (390)?

Appropriate clarification/correction is required.

Claim Objections

3. Claims 1 and 3 are objected to for the following reasons.

Referring to Claim 1: Claim 1 is a product claim and, therefore, is objected to because it uses claim language that includes a manipulative step, which is proper process claim language.

Referring to Claim 3: Claim 3 refers back to the method of Claim 1. Claim 1 is not a process claim, it is a product claim, namely a chip scale package (CSP).. Appropriate correction is required.

Claim Rejections 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

5. Claims 1, 5, and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over U. S. Patent Application Publication No. US 2001/0021541, Application No. 09/832,160 (Akram *et al.*) The figures and reference numbers referred to in this office action are used merely to indicate examples of specific teachings and are not to be taken as limiting.

Referring to Claim 1: Akram *et al.* disclose a CSP (chip-scale package) (Figure 1 (10)) comprising:

a silicon chip having I/O pads (although, Akram does not specifically disclose a silicon chip, he does disclose having a "semiconductor device" (12) having bonding pads (16) in the first two lines of paragraph [0048] and teaches in the fourth line of [0005] that it is conventional to use silicon wafers, therefore, as silicon was one of the most widely used materials with which to fabricate chips at the time of the invention and as this fact was well known by those of ordinary skill in the art at that time, it would have been obvious to provide for a chip of silicon);

an under-ball metallurgy (UBM) layer on the surface of said I/O pads (UBM is discussed in the last sentence of [0068]);

a substrate (Figure 1 (18)) with an adhesive (the "ad-substrate" of the present Application) (the application of an adhesive to the substrate is disclosed in the second sentence of [0052]) and having openings corresponding to the locations of said I/O pads (Figure 1 (21); and

ball mountings (i.e., balls or bumps) (Figure 1 (24)) formed over said ad-substrate and reaching said UBM layer (an example of UBM mountings is shown in Figure 6 (23)) over said I/O pads (Figure 6 (21)) on said chip (Figure 6 (12)).

Referring to Claim 5: Akram *et al.* disclose a CSP, as recited above, further disclosing wherein said substrate comprises a ball grid array (BGA) (bond pads in an array is taught in the third line of [0048]; the arrangement of vias in correspondence with the bond pads is taught in the second sentence of [0049]; and that conductive bumps are disposed in communication with corresponding electrically conductive vias is taught is lines 15 – 17 of [0049]).

Referring to Claim 9: Akram *et al.* disclose a CSP, as recited above, further disclosing wherein said I/O pads comprise an area array (AA) or are redistributed to form a redistribution layer (see discussion of redistribution of bond pads (16) via traces (22) in last sentence of [0062]).

6. Claims 2 and 3 are rejected under 35 U.S.C. 103(a) as being unpatentable over United States Patent Application Publication No. US 2001/0021541, Application No. 09/832,160 (Akram *et al.*) in view of United States Patent No. 5,846,875 (Haji).

Referring to Claim 2: Akram *et al.* disclose a CSP, as recited above, except for explicitly disclosing wherein said first layer of I/O pads comprise aluminum alloy or copper.

Haji discloses wherein said first layer of I/O pads comprise aluminum (Haji, Col. 3, line 16).

It would have been obvious to one of ordinary skill in the art at the time the invention was made o modify the CSP disclosed by Akram *et al.* by providing a first layer of I/O pads comprising aluminum alloy or copper as disclosed by Haji as it was very well know to use either of these materials as bond pads. Copper especially, is an excellent conductor and is the most widely used materials for conduction material purposes.

Referring to Claim 3: Akram *et al.* disclose a CSP, as recited above, except for explicitly disclosing wherein the UBM (under bump metallurgy) layer comprises nickel or copper.

Haji discloses wherein the UBM layer comprises nickel or copper (Haji, Col. 5, lines 47 - 53).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the CSP disclosed by Akram *et al.* by providing a UBM layer comprising nickel or copper as disclosed by Haji as it was well know to use either of these materials as under-bump metals as both metals have a coefficient of thermal expansion similar to that of aluminum (Haji, Col. 4, line 66 – Col. 5, line 1) and will both provide for good adhesion to the aluminum (see, Haji, Col. 5, lines 22 – 23 in conjunction with Col. 5, lines 47 - 53).

7. Claims 4 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over United States Patent Application Publication No. US 2001/0021541, Application No. 09/832,160 (Akram *et al.*) in view of United States Patent No. 6,265,782 (Yamamoto *et al.*).

Referring to Claim 4: Akram *et al.* disclose a CSP, as recited above, except for explicitly disclosing wherein the substrate comprises bismaleimide triazine (BT).

Yamamoto *et al.* discloses wherein the substrate comprises bismaleimide triazine (BT) (Yamamoto *et al.*, Col. 8, lines 62 – 63).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the CSP disclosed by Akram *et al.* by providing for a substrate comprising bismaleimide triazine (BT) as disclosed by Yamamoto *et al.* as BT was a conventional material, well known by those of ordinary skill in the art, with which substrates for BGA (ball grid array) packages were made (note: BGA type packages are a sort of CSP, as is admitted by the present Application).

Referring to Claim 6: Akram *et al.* disclose a CSP, as recited above, further disclosing wherein said substrate has a thickness between about 150 to 300 microns (lines 17 and 18 of [0053]).

Akram *et al.* do not explicitly disclose and wherein said adhesive has a thickness between about 10 to 100 microns.

Yamamoto *et al.* discloses an adhesive layer having a thickness between about 10 to 100 microns (Yamamoto *et al.*, Col. 16, lines 51 - 55.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the proposed device of Akram *et al.* by providing for an adhesive layer having a thickness between about 10 to 100 microns as disclosed by Yamamoto *et al.* to obtain the advantage of having an layer with a thickness not so thin that the layer " . . . may have a poor adhesion or thermal stress relaxation effect," or a layer with " . . . a thickness . . . [that] is not economical . . ." (Col. 16, lines 52 – 55). Additionally, it would have been obvious at the time of the invention by one of ordinary skill in the art to provide for an adhesive of between about 10 to 100 microns as it was, and still is, reasonable to

use a layer of adhesive that has a substantially lesser thickness than that which the adhesive is adhering (to use more would incur waste and excess adhesive to contaminate other parts of the device), wherein it is also reasonable to use a not too thin layer, such as less than about 10 microns as the adhesion would be weak.

Additionally, Applicant has not supplied any reason why the recited range given for the thickness of the adhesive is functionally critical to the invention.

8. Claims 7 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over U. S. Patent Application Publication No. US 2001/0021541, Application No. 09/832,160 (Akram *et al.*) in view of United States Patent No. 5,480,835 (Carney *et al.*)

Referring to Claim 7: Akram *et al.* disclose a CSP, as recited above, except for explicitly disclosing wherein the ball mountings (note: ball mountings are understood by Examiner to be the same as "solder balls" or "solder bumps") comprise tin-lead or tin-silver alloy.

Carney *et al.* discloses wherein the ball mountings comprise tin-lead or tin-silver alloy:

> An interconnect material, for example, solder has well known adhesive qualities suitable for mechanical coupling to a pad. Solder is also electrically conductive. Solder is an alloy commonly formed from a combination of tin-lead, many other solder alloys exist such as tin-bismuth, indium-tin, tin-lead-silver, and tin-gold to name only a few. Although solder is the preferred embodiment of the interconnect material, any

> electrically conductive material having similar properties as described herein will suffice as an alternate to solder (from Carney *et al.*, Col. 3, lines 19 - 39) (emphasis added).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the CSP disclosed by Akram *et al.* by providing for ball mountings comprising tin-lead alloy as disclosed by Carney *et al.* as lead/tin was well known by those of ordinary skill in the art, as a conventional material to use in the formation of interconnect materials, such as "solder balls" or "solder bumps" to interconnect vias in a CSP substrate to a mother board, for example.

Referring to Claim 8: Akram *et al.* disclose a CSP, as recited above, except for explicitly disclosing wherein the ball mountings (note: ball mountings are understood by Examiner to be the same as "solder balls" or "solder bumps") have a height between about 300 to 800 microns.

Carney *et al.* discloses wherein the ball mountings have a height between about 300 to 800 microns:

> The height of interconnect ball 74 is a function of the area of wettable surface 73 and the total volume of interconnect material. The surface tension of solder is such that solder balls having heights in excess of 100 microns can be formed using this technique. (from Carney *et al.*, Col. 6, lines 18 –22) (emphasis added).

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the CSP disclosed by Akram *et al.* by providing for ball

mountings with a height of about 300 to 800 microns as disclosed by Carney *et al.*, because as Carney *et al.* state: "solder ball . . height[s] are critical to producing reliable interconnection[s]" (Col. 1, lines 19 — 23).

9. Claims 10 - 16, 18, 19, 22 – 27, and 31 are rejected under 35 U.S.C. 103(a) as being unpatentable over U. S. Patent Application Publication No. US 2001/0021541, Application No. 09/832,160 (Akram *et al.*) in view of United States Patent No. 6,355,507 (Fanworth)).

Referring to Claim 10: Akram *et al.* disclose a CSP, as recited above, except for explicitly disclosing wherein the CSP is encapsulated in a molding material comprising epoxy resin.

Fanworth does explicitly teach forming a molding material comprising epoxy resin to encapsulate a CSP (see Fanworth, Abstract and Col. 6, lines 40 - 47).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the CSP disclosed by Akram et al. by providing for a molding material around said package as taught by Fanworth as it was well known in the art to do so and, in addition, to obtain the advantage of providing for a chip that is protected from hazards presented in its immediate environment, such as moisture, contaminants, and stress.

Referring to Claim 11: Akram *et al.* disclose a method of forming a CSP (chip-scale package) comprising the steps of:

providing one or more chips (Figure 1 (12)) having I/O pads (Figure 6 (16)) with UBM layer (Figure 6 (23)) on the surface of said I/O pads;

providing a substrate (Figure 1A (118));

applying an adhesive layer over said substrate (see second sentence of paragraph [0052]) thus forming an ad-substrate composite;

forming openings (Figure 1 (21)) in said ad-substrate composite to match the spacing of corresponding said I/O pads (Figure 1 (16)) of said chip);

attaching said chip(s) on said ad-substrate composite wherein said I/O pads of said chip(s) are placed on the corresponding openings on said ad-substrate composite to form a package (CSP package (10) as illustrated in Figure 1);

performing ball mounting over said openings on said ad-substrate of said package (Figure 1 (22) and (24)); and

forming said CSP.

Akram et al. does not explicitly teach forming a molding material around said package.

Fanworth does explicitly teach forming a molding material around said package (Fanworth, Figure 4 (32) and Col. 6, lines 30 –35) (see discussion for Claim 10, above).

Referring to Claims 12 – 16, 18, 22, 24, 25, 27: The proposed device of Akram *et al.* and Fanworth discloses a method of forming a CSP, as recited above, including the limitation of Claims 12 – 16,

Referring to Claim 19: The proposed device of Akram *et al.* and Fanworth discloses a method of forming a CSP, as recited above, further disclosing wherein forming said openings is accomplished by mechanical or laser drilling, or screen printing (Akram *et al.*, first sentence, paragraph [0084].

Referring to Claim 23: The proposed device of Akram et al. and Fanworth discloses a method of forming a CSP, as recited above, except for explicitly disclosing wherein said molding material has a thickness between about 100 to 500 micron.

It would have been obvious, however, to one of ordinary skill in the art at the time the invention was made to modify the proposed device of Akram et al. and Fanworth to provide for a molding material having a thickness of between about 100 to 500 microns for the reasons that follow.

As stated by Fanworth in Col. 7, lines 54 – 59, the encapsulant envelope may have any desired thickness on all the surfaces of the die except for the active surface, which includes balls or bumps. The thickness of the encapsulant envelope on the active surface must be less than the height of balls, to allow for subsequent connection to a carrier substrate.

The present Application recites ball mountings having a height of between about 300 to 800 microns (Claims 8 and 25) thus, the molding material height on the active surface (i.e., the surface having the ball mountings) must have been less than 300 to 800 microns. Therefore, it was obvious to have a molding material thickness on the active surface of between about 100 to 500 microns to

provide protection to the active surface of the chip while providing for electrical connection to another device, such as a motherboard.

Referring to Claim 26: The proposed device of Akram *et al.* and Fanworth discloses a method of forming a CSP, as recited above, further disclosing wherein forming said package comprises:

a wafer (Akram *et al.*, Figure 2B) having a plurality of chip sites with I/O pads (as taught by Akram *et al.* in paragraph [0058]);

Referring to Claim 31: The proposed device of Akram *et al.* and Fanworth discloses a method of forming a CSP, as recited above, further disclosing where forming said adhesive layer over said UBM layer comprises lamination, spin coating, or screen printing (Akram *et al.*, last one-third of paragraph [0079]).

10. Claims 17 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over United States Patent Application Publication No. U.S. 2001/0021541, Application No. 09/832,160 (Akram *et al.*) in view of United States Patent No. 6,355,507 (Fanworth) further in view of United States Patent No. 6,265,782 (Yamamoto *et al*).

Referring to Claim 17: The proposed device of Akram et al. and Fanworth discloses a method of forming a CSP, as recited above, except for explicitly disclosing wherein the adhesive layer comprises polyimide thermo-compression adhesive.

Yamamoto *et al.* discloses an adhesive layer comprising polyimide thermo-compression adhesive (Yamamoto *et al.*, Col. 3, lines 53 – 57 and Col. 5, line 56 – 59).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the proposed device of Akram et al. and Fanworth by providing the adhesive layer comprises polyimide thermo-compression adhesive as disclosed by Yamamoto *et al.* to obtain the advantage of having:

> an adhesive and an adhesive film which have thermal resistance, electrolytic corrosion resistance and moisture resistance required when semiconductor chips having a great difference in coefficient of thermal expansion are packaged on printed-wiring boards such as glass epoxy substrates or flexible substrates, and especially may less cause a deterioration when tested on moisture resistance under severe conditions as in PCT treatment or the like, and provides a semiconductor device in which a semiconductor chip has been bonded to a wiring board by the use of such an adhesive film (Yamamoto *et al.* Col. 2, line 63 - Col. 3, line 6).

Referring to Claim 21: The proposed device of Akram et al. and Fanworth discloses a method of forming a CSP, as recited above, except for explicitly disclosing wherein said attaching said chip(s) is accomplished by subjecting said ad-substrate to a temperature between about 250 to 350°C at a pressure between about 1.5 to 2.5 Megapascals.

Yamamoto *et al.* discloses wherein said attaching said chip(s) is accomplished by subjecting said ad-substrate to a temperature between about 250 to 350°C at a pressure between about 1.5 to 2.5 Mpa (Col. 9, lines 31 – 33 and 42 - 44).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the proposed device of Akram *et al.* and Fanworth by attaching said chip(s) is accomplished by subjecting said ad-substrate to a temperature between about 250 to 350°C at a pressure between about 1.5 to 2.5 Mpa as disclosed by Yamamoto *et al.* to obtain the advantage of having a satisfactory bond. As discussed by Yamamoto *et al.*, in Col. 9, lines 34 – 40, if the temperature is too low adhesion will occur and the adhesive will not fill the space of bonding. If the temperature is too high, the wiring may be oxidized.

11. Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over U. S. Patent Application Publication No. US 2001/0021541, Application No. 09/832,160 (Akram *et al.*) in view of United States Patent No. 6,355,507 (Fanworth) further in view of United States Patent No. 6,232,247 (Matsuki *et al.*).

Akram *et al.* disclose a method of forming a CSP as recited above except for explicitly disclosing wherein the apertures or openings have a diameter between about 350 to 900 microns.

Matsuki *et al.* disclose apertures or openings have a diameter between about 350 to 900 microns (Matsuki *et al.*, Col. 12, lines 66 – 67).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the method disclosed by Akram et al. by providing for apertures or openings having a diameter between about 350 to 900 microns as disclosed by Matsuki *et al.* to obtain the advantage of having the claimed ball mountings fit into their corresponding apertures.

12. Claims 28 – 30 and 32 – 41 are rejected based on the reasoning given above as the limitations of Claim 28 – 30 and 32 – 41 have all been recited and discussed above.

Conclusion

Any inquiry concerning this communication should be directed to Patricia Costanzo at 703 305-5675 on Monday – Friday from 8:00 A.M. – 5:00 P.M.

If attempts to reach the examiner by telephone are unsuccessful Supervisory Primary Examiner Tom Thomas can be reached at 703 308 -2772.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group Receptionist at 703 308-0956.

Using facsimile machines to transmit correspondence is encouraged. The official Technical Center 2800 before-final FAX number is 703-872-9318 and the after-final FAX number is 703-872-9319. These FAX numbers will provide the FAX sender with an auto-reply verifying receipt of their FAX by the United States Patent and Trademark Office. If there should be a problem while faxing to the Office, please contact Technical Center 2800 Customer Service at 703-306-3329.

pmc
May 28, 2002

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